**Practical No.1**

**Logic Gates Truth Table Verification:**

**Study and verify the truth table of various logic gates (NOT, AND, OR, NAND, NOR, EX-OR, EX-NOR) using Logisim.**

### 1] NOT Gate (Inverter): Inverts the input

| A | Output (A̅) |
| --- | --- |
| 0 | 1 |
| 1 | 0 |

**2] AND Gate : Output is true only if all inputs are true**

| A | B | A ⋅ B |
| --- | --- | --- |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**Concept:** Output is 1 only if **both** inputs are 1

### 3]. OR Gate: Output is true if at least one input is true

| A | B | A + B |
| --- | --- | --- |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

### 4]. NAND Gate : Inverse of AND

| A | B | ¬(A ⋅ B) |
| --- | --- | --- |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**5]. NOR Gate :** Inverse of OR

| A | B | ¬(A + B) |
| --- | --- | --- |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**6].XOR Gate (Exclusive OR):** Output is true if inputs are different

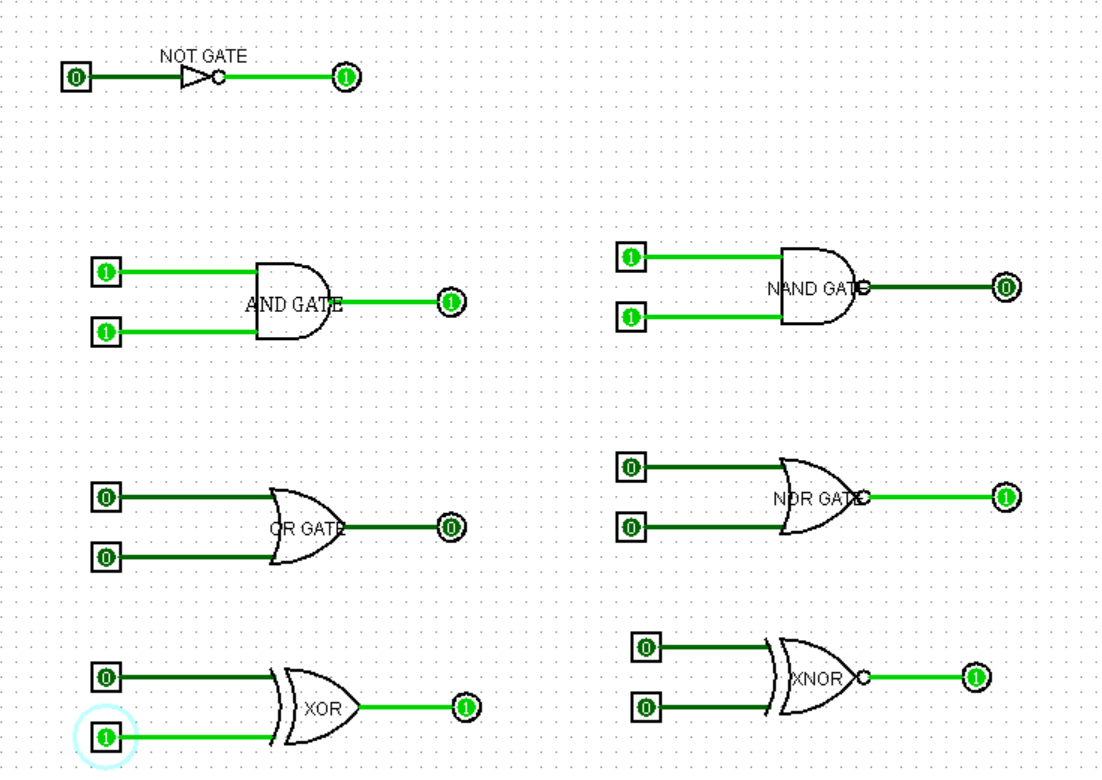
| A | B | A ⊕ B |
| --- | --- | --- |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**7].XNOR Gate**: Output is true if inputs are the same

| A | B | ¬(A ⊕ B) |
| --- | --- | --- |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

* **Digital door lock**: Door unlocks if **entered password = stored password**

**O/P**



**Practical No.2**

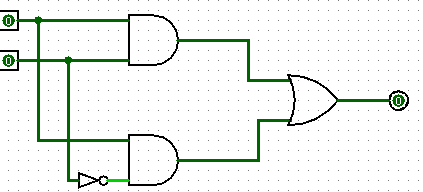
**A. Definition And Simplification**

**B. Realize in Logisim**

**C. K-map / SOP Confirmation**

**Conclusion:** The original circuit is redundant — the output depends only on A.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **A⋅B** | **A⋅B′** | **Y=A⋅B+A⋅B′Y '** | **equals A?** |  |
| 0 | 0 | 0 | 0 | 0 | 0 |  |
| 0 | 1 | 0 | 0 | 0 | 0 |  |
| 1 | 0 | 0 | 1 | 1 | 1 |  |
| 1 | 1 | 1 | 0 | 1 | 1 |  |



**Practical No.3**

**What is an Adder?**

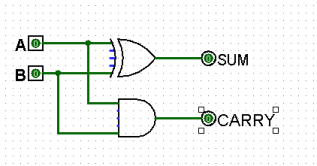
An adder is a kind of calculator that is used to add two binary numbers. When I say, calculator, I don’t mean one with buttons, this one is a circuit that can be integrated with many other circuits for a wide range of applications. There are two kinds of adders;

1. Half adder

2. Full adder

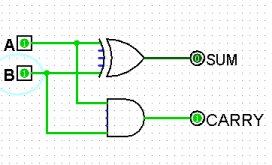
**Half Adder**

With the help of half adder, we can design circuits that are capable of performing simple addition with the help of logic gates.

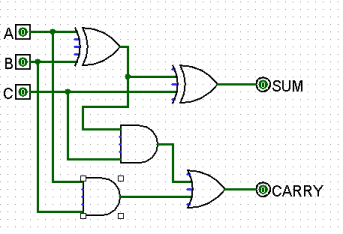


The 2-bit **half adder truth table** is as below:

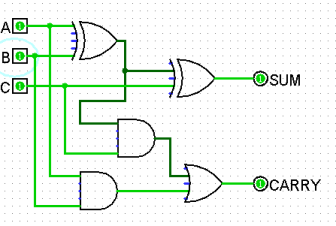
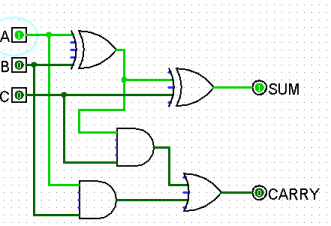
|  |  |  |  |
| --- | --- | --- | --- |
| A | B | SUM | CARRY |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

**Full Adder**

This type of adder is a little more difficult to implement than a half-adder. The main difference between a half-adder and a full-adder is that the full-adder has three inputs and two outputs. The first two inputs are A and B and the third input is an input carry designated as CIN. The output carry is designated as COUT and the normal output is designated as S./



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | SUM | CARRY |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |



**Practical No.4**

**1.Subtractor**

**2.Half Subtractor**

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | Difference(D) | Borrow(Bout) |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

A diagram of a circuit

AI-generated content may be incorrect.

**3.Full Subtractor**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **Bin** | **Difference (D)** | **Borrow (Bout)** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

A diagram of a circuit

AI-generated content may be incorrect.

**Practical No.5**

A.MAGNITUDE COMPARATOR IN DIGITAL LOGIC

A white rectangular object with green text

AI-generated content may be incorrect.

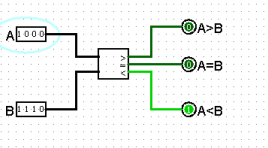
B. 4 BIT MAGNITUDE COMPARATOR:

A diagram of a circuit

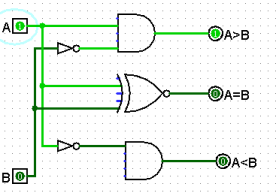
AI-generated content may be incorrect.

A diagram of a circuit

AI-generated content may be incorrect.



**C. 1 BIT MAGNITUDE COMPARATOR:**



A diagram of a circuit

AI-generated content may be incorrect.

A diagram of a circuit

AI-generated content may be incorrect.

**Practical No.6**

**SR flip flop**

A diagram of a circuit

AI-generated content may be incorrect.A diagram of a circuit

AI-generated content may be incorrect.

A diagram of a circuit

AI-generated content may be incorrect.

SR Flip Flop Clocked

A diagram of a block diagram

AI-generated content may be incorrect.

A diagram of a circuit

AI-generated content may be incorrect.

**JK Flip Flop**

A table with text on it

AI-generated content may be incorrect.

**Practical No.7**

**A.Design 4-Bit Magnitude Comparator in Logisim**

A table with numbers and symbols

AI-generated content may be incorrect.

======================

A diagram of a circuit diagram

AI-generated content may be incorrect.

**B.Logic diagram using T flip-flop is shown in Fig**

**C.4 BIT SYNCHRONOUS (UP) COUNTER**

A diagram of a block diagram

AI-generated content may be incorrect.

A diagram of a block diagram

AI-generated content may be incorrect.

**D.4 BIT ASYNCHRONOUS (DOWN) COUNTER:**

A diagram of a diagram

AI-generated content may be incorrect.A diagram of a diagram

AI-generated content may be incorrect.

**Practical No.8**

**A.What is a 4-bit Shift Register?**

Example:

Suppose we input 1011 serially:

Clock Input Q3 Q2 Q1 Q0

1 1 0 0 0 1

2 0 0 0 1 0

3 1 0 1 0 14 1 1 0 1 1

**4 BIT SHIFTER:**

**The Shift Register**

A diagram of a network

AI-generated content may be incorrect.

A green line with black squares and black dots

AI-generated content may be incorrect.

**Practical No.9**

**AIM:Design and implement a 3-bit binary ripple counter**

Using Multiplexers/Demultiplexers

**Multiplexer:-**

A screenshot of a computer

AI-generated content may be incorrect.

**Demultiplexer:-**

A computer screen shot of a computer network

AI-generated content may be incorrect.